2008 VLSI Circuits Short Course

This year the Circuits Short Course is comprised of two programs, Memory and Analog/Digital. The cost of the short course includes both programs and attendees will receive one book for both programs. Attendees will be able to move back and forth between the two programs.

Memory Short Course Program
Embedded Memory Design

Honolulu I
Tuesday, June 17, 8:10 a.m.

Organizers/Chairs: John Barth, IBM
Masao Ito, Renesas Technology Corporation

8:10 a.m.	**Introduction** J. Barth, IBM
8:15 a.m.	**Embedded Memory Overview (and DRAM)** S. Natarajan, TSMC Design Technology Canada
9:25 a.m.	**Static RAM** M. Yamaoka, Hitachi, Ltd.
10:35 a.m.	**Break**
10:50 a.m.	**Floating Body RAM** T. Ohsawa, Toshiba Corporation
12:00 p.m.	**Lunch**
1:30 p.m.	**Phase Change RAM** C. Lam, IBM
2:40 p.m.	**Break**
2:55 p.m.	**Flash** R. Kakoschke, Infineon
4:05 p.m.	**Built in Self Test**

D. Weiss, AMD

5:15 p.m. **Conclusion**
M. Ito, Renesas Technology Corporation

Analog/Digital Short Course Program
Embedded Power Management Circuits and Systems

Honolulu II
Tuesday, June 17, 8:10 a.m.

Organizers/Chairs: Tom Kwan, Broadcom Corporation
Koichi Nose, NEC Corporation

8:10 a.m. **Introduction**
T. Kwan, Broadcom Corporation

8:15 a.m. **Overview of Embedded Power Management Circuits and Systems in SoC's**
D. Anderson, National Semiconductor Corp.

9:25 a.m. **Integrated Power Management for Mobile SoC's**
D. Ho, Broadcom Corporation

10:35 a.m. **Break**

10:50 a.m. **Circuit Design for Power Management Building Blocks**
W.-H. Ki, Hong Kong University of Science and Technology

12:00 p.m. **Lunch**

1:30 p.m. **Thermal Management of High-Performance Processors**
E. Miranda, Analog Devices Corp.

2:40 p.m. **Break**

2:55 p.m. **Power Management at the System/Architecture/Circuit Level**
M. Nomura, NEC

4:05 p.m. **Dynamic Power/Thermal Management in High Performance Processors; Examples and Opportunities**
S. Naffziger, AMD

5:15 p.m. **Speaker Interview Session**

SESSION 1 – TAPA II
Plenary Session

Wednesday, June 18, 8:25 a.m.
Chairpersons: K. Nakamura, Analog Devices Inc.
M. Mizuno, NEC Corporation

8:25 a.m. **Welcome and Opening Remarks**
S. Kosonocky, AMD
K. Yano, Hitachi Ltd.

1.1 – 8:40 a.m.
Next Generation Micro-Power Systems
A.P. Chandrakasan, D.C. Daly, J. Kwong, Y.K. Ramadass,
Massachusetts Institute of Technology

Emerging microsystems such as portable and implantable medical electronics, wireless microsensors and next-generation battery-operated multimedia devices demand a dramatic reduction in energy consumption. The ultimate goal is to power these devices using energy harvesting techniques such as vibration-to-electric conversion or through wireless power transmission. A major opportunity to reduce the power dissipation of digital circuits is to scale supply voltages to 0.5V and below. The challenges associated with ultra-low-voltage design in scaled technologies will be presented. This includes variation-aware design for logic and SRAM circuits, efficient DC-DC converters for ultra-low-voltage delivery, and algorithm structuring to support extreme parallelism. Micro-power analog and RF circuits require the use of application-specific structures as well as digital and variation-aware architectures to leverage process scaling.

1.2 – 9:25 a.m.
Power-Efficient Heterogeneous Parallelism for Digital Convergence
K. Uchiyama, Hitachi, Ltd.

For embedded systems in the digital-convergence era, various functions such as communication, security, audio, video, and recognition, are required in a single device. However, improving the speed of an embedded LSI in the system is

difficult because of the significantly increasing power-consumption problems. Heterogeneous parallelism on an SoC has been studied to solve these problems. A power-thrifty architecture, which combines embedded CPUs and special processing cores such as dynamic reconfigurable processors, has been proposed targeting a superior performance per power ratio and functional flexibility. From the viewpoint of programming, a parallelizing compiler and an Application Program Interface (API) have been developed that are suitable for heterogeneous parallelism. The evaluation results of various applications tested using prototype chips and programs will also be discuss ed.

10:10 a.m. Break

SESSION 2 –TAPA I
High-Speed Data Converters

Wednesday, June 18, 10:25 a.m.
Chairpersons: B. Nauta, University of Twente
M. Nagata, Kobe University

2.1 – 10:25 a.m.
A Low Power 6-bit Flash ADC with Reference Voltage and Common-Mode Calibration, C.-Y. Chen, M. Le, K.Y. Kim, Broadcom Corporation, USA

A low power 6-bit ADC that uses reference voltage and common-mode calibration to improve linearity and reduce power dissipation is presented. The ADC occupies 0.13mm2 in 65nm CMOS. The ADC dissipates 4mW at 100MS/s and 12mW at 800MS/s from a 1.2V supply.

2.2 – 10:50 a.m.
A 7.6 mW 1.75 GS/s 5 Bit Flash A/D Converter In 90nm Digital CMOS, B. Verbruggen, P. Wambacq, M. Kuijk*, G. Van der Plas, IMEC, *Vrije Universiteit, Belgium

A 5 bit 1.75 GS/s flash ADC is realized in 90 nm CMOS. It uses a comparator array with built-in imbalance and offset calibration to lower power consumption. The SNDR is 30.9 dB at low frequencies and gradually degrades to 28.2 dB at 2 GHz. The ADC occupies 280µm by 110µm and draws only 7.6 mA from a 1 V supply yielding an energy efficiency of 0.15 pJ/conversion step.

2.3 – 11:15 a.m.
A 6-bit 5-GSample/s Nyquist A/D Converter in 65nm CMOS, M. Choi, J. Lee, J. Lee, H. Son, Samsung Advanced Institute of Technology, Korea

A 6-bit Nyquist A/D converter (ADC) that converts at 5 GHz is reported. Using a wideband track-and-hold amplifier, array averaging, reset switches on analog signal paths, and phase-adjusted clocking for cascaded comparators, a 6-bit flash ADC achieves better than 5 effective bits for input frequencies up to 2.5 GHz at 5 GSample/s. This ADC does not rely on time interleaving, digital calibration, and post data processing for its dynamic performance. This ADC consumes about 320mW from 1.3 V at 5 GSample/s. The chip occupies 0.3mm2 active area, fabricated in 65nm CMOS.

2.4 – 11:40 a.m.

A 10.3GS/s 6bit (5.1 ENOB at Nyquist) Time-Interleaved/Pipelined ADC Using Open-Loop Amplifiers and Digital Calibration in 90nm CMOS, A. Nazemi, C. Grace, L. Lewyn, B. Kobeissy, O. Agazzi, P. Voois, C. Abidin, G. Eaton, M. Kargar, C. Marquez, S. Ramprasad, F. Bollo*, V. Posse, S. Wang, G. Asmanis, ClariPhy Communications Inc., USA, *ClariPhy, Argentina

A 10.3GS/s ADC with 5GHz input BW and 6 bit resolution in 90nm CMOS is presented. The architecture is based on an 8 way interleaved/ pipelined ADC using open-loop amplifiers and digital calibration. The measured performance is 5.8 ENOB (36.6dB SNDR) for a 100MHz input signal and 5.1 ENOB (32.4dB SNDR) for a 5GHz input (Nyquist) with phase offset correction across the interleaved array.

12:05 p.m. Lunch

SPECIAL SESSION – TAPA II
Technology Highlights

Wednesday, June 18, 10:25 a.m.
Chairpersons: C. Dennison, Ovonyx Technologies
M. Niwa, Matsushita Electric Ind. Co.

9.1 - 10:25 a.m.

Fully Integrated and Functioned 44nm DRAM Technology for 1GB DRAM, H. Lee, D.-Y. Kim, B.-H. Choi, G.-S. Cho, S.-W. Chung, W.-S. Kim, M.-S. Chang, Y.-S. Kim, J. Kim, H.-J. Lee, H.-S. Song, S.-K. Park, J.-W. Kim, S.-J. Hong, S.-W. Park, Hynix Semiconductor, Korea

9.2 - 10:50 a.m.

A Cost Effective 32nm High-K/ Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process, X. Chen, S. Samavedam*, V. Narayanan, K. Stein, C. Hobbs*, C. Baiocco, W. Li, D. Jaeger, M. Zaleski*, S. Yang, N. Kim**, Y. Lee, D. Zhang*, L. Kang*, J. Chen**, H. Zhuang^, A. Sheikh, J. Wallner, M. Aquilino, J. Han^, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kershnan, Z. Wang, M. Chudzik, M. Chowdhury*, D. Nair, C. Reddy*, Y.W. Teh**, C. Kothandaraman, D. Coolbaugh, S. Pandey**, D. Tekleab**, A. Thean*, M. Sherony, C. Lage*, J. Sudijono**, R. Lindsay^, J.-H. Ku^^, M. Khare, A. Steegen, IBM SDRC, *Freescale Semiconductor, **Chartered Semiconductor Manufacturing, ^Infineon Technologies, ^^Samsung Electronics Co., USA

9.3 - 11:15 a.m.

Variability Aware Modeling and Characterization in Standard Cell in 45nm CMOS with Stress Enhancement Technique, H. Aikawa, E. Morifuji, T. Sanuki, T. Sawada, S. Kyoh, A. Sakata, M. Ohta, H. Yoshimura, T. Nakayama, M. Iwai, F. Matsuoka, Toshiba Corp. Semicoductor Company, Japan

9.4 - 11:40 a.m.
A Scaled Floating Body Cell (FBC) Memory with High-k+Metal Gate on Thin-Silicon and Thin-BOX for 16-nm Technology Node and Beyond, I. Ban, U. Avci, D. Kencke, P. Chang, Intel Corporation, USA

12:05 p.m. Lunch

SESSION 3 – TAPA II
Parallel Processing

Wednesday, June 18, 1:30 p.m.
Chairpersons: J. Farrell, AMD
K. Kobayashi, Kyoto University

3.1 – 1:30 p.m.
A 167-processor 65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling, D. Truong, W. Cheng, T. Mohsenin, Z. Yu, T. Jacobson, G. Landge, M. Meeuwsen, C. Watnik, P. Mejia, A. Tran, J. Webb, E. Work, Z. Xiao, B. Baas, University of California, Davis, USA

A 167-processor 65 nm computational platform well suited for DSP, communication, and multimedia workloads contains 164 programmable processors with dynamic supply voltage and dynamic clock frequency circuits, 3 algorithm-specific processors, and 3 16 KB shared memories, all clocked by independent oscillators and connected by configurable long-distance-capable links.

3.2 – 1:55 p.m.
A 26mW 6.4GFLOPS Multi-Core Stream Processor for Mobile Multimedia Applications, Y.-M. Tsao, C.-H. Sun, Y.-C. Lin, K.-H. Lok, C.-J. Hsu*, S.-Y. Chien, L.-G. Chen, National Taiwan University, Taiwan, *UMC, Taiwan

A 26mW 6.4GFLOPS multi-core stream processor for mobile applications is implemented in 90nm CMOS technology. A unified stream processing architecture with power-aware frequency scaling and adaptive task scheduling techniques are proposed to reduce the power consumption and increase the performance to achieve the performance of 200Mvertices/s and 400Mpixels/s in 3D graphic applications.

3.3 – 2:20 p.m
The Brain Mimicking Visual Attention Engine: An 80x60 Digital Cellular Neural Network for Rapid Global Feature Extraction, S. Lee, K. Kim, M. Kim, J.-Y. Kim, H.-J. Yoo, KAIST, Korea

The Visual Attention Engine(VAE), an 80x60 digital Cellular Neural Network, rapidly extracts global features used as attentional cues to streamline detailed object recognition. A peak performance of 24GOPS is achieved by 120 processing elements (PE) shared by the cells. 2D Shift register based data transactions enable 93% PE utilization. Integrated within an object recognition SoC, the 4.5mm2 VAE running at 200MHz improves object recognition frame rate by 83% while consuming just 84mW.

3.4 – 2:45 p.m.
A 100 GOPS In-vehicle Vision Processor for Pre-crash Safety Systems Based on a Ring Connected 128 4-Way VLIW Processing Elements, S. Kyo, S. Okazaki, T. Koga*, F. Hidano*, NEC Corporation, Japan, *NEC Electronics Corporation, Japan

A 100GOPS vision processor LSI (IMAPCAR) for in-vehicle image recognition which consumes less than 2 watts of power has been developed. 128 of 4-Way VLIW with MAC (multiply add accumulation) processor elements (PE) to which data are assigned efficiently by DMA companion scaling capability, has achieved high performance in low cost. Compared with a previous design, performance for major vision tasks has been improved by a factor of 2.5 while 50% of power is reduced.

3:10 p.m. **Break**

SESSION 4 – TAPA III
Low-Power and Reconfigurable RF

Wednesday, June 18, 1:30 p.m.
Chairpersons: A. Abidi, University of California, Los Angeles
H. Ishikuro, Keio University

4.1 – 1:30 p.m.
A 350uW CMOS MSK Transmitter and 400uW OOK Super-Regenerative Receiver for Medical Implant Communications, J.L. Bohorquez, J.L. Dawson, A.P. Chandrakasan, Massachusetts Inst. of Tech, USA

A 350μW MSK direct modulation transmitter and 400μW OOK super-regenerative receiver are implemented in 90nm CMOS technology. The transceiver tunes 24MHz in frequency steps smaller than 2kHz and is optimized for the Medical Implant Communications Service (MICS) standard in the 402--405MHz band. The transmitter meets MICS mask specifications with data rates up to 120kbps, and the receiver has a sensitivity better than -99dBm with a data rate of 40kbps or -93dBm with a data rate of 120kbps.

4.2 – 1:55 p.m.
A 5GHz Fully Integrated Super-regenerative Receiver with On-chip Slot Antenna in 0.13μm CMOS, D. Shi, N. Behdad*, J.-Y. Chen**, M. Flynn, University of Michigan, *University of Central Florida, **ZeroG Wireless Inc., USA

A super-regenerative receiver with a novel on-chip slot antenna and a compact capacitively-loaded standing-wave resonator is reported. An all-digital PLL synchronizes the received data clock. The prototype 5GHz receiver, implemented in 0.13μm CMOS, achieves a highest data rate of 1.2Mb/s, dissipates 6.6mW from a 1.5V supply, and occupies a die area of 2.4mm2

4.3 – 2:20 p.m.

A Direct Conversion Receiver Adopting Balanced Three-phase Analog System, T. Yamaji, T. Itakura, T. Ueno, Toshiba Corporation, Japan

A new wireless receiver architecture that has small analog area is proposed and evaluation of the core analog blocks is described. To reduce the analog area, a balanced 3-phase analog system is adopted and the functions of analog baseband filters and VGAs are moved to digital domain. The downconverter and ADC are directly connected and they occupy 0.28 mm2.

4.4 – 2:45 p.m.
A Direct-Conversion CMOS RF Receiver Reconfigurable from 2GHz to 6GHz, J. Park, S.-N. Kim, J.-H. Seok, Y.-S. Roh, C. Yoo, K. Lim*, J. Kim*, Hanyang University, Korea, *Future Communications IC Inc., Korea

A CMOS direct-conversion receiver with only one signal path is reconfigurable from 2GHz to 6GHz in the RF band and from 3.6MHz to 54MHz in the channel bandwidth. By employing a voltage feedback in a common-gate low-noise amplifier (LNA), the input matching of the LNA can be reconfigured for each RF band by simply changing the resonant frequency of load network. Implemented in a 0.18μm 1P5M RF CMOS technology, the whole receive path shows 4.6~5.6dB noise figure.

3:10 p.m. Break

SESSION 5 – TAPA II
SRAM Variability

Wednesday, June 18, 3:25 p.m.
Chairpersons: A. Bhavnagarwala, IBM TJ Watson Research Ctr.
T. Sekiguchi, Hitachi, Ltd.

5.1 – 3:25 p.m.
Large-Scale Read/Write Margin Measurement in 45nm CMOS SRAM Arrays, Z. Guo, A. Carlson, L.-T. Pang, K. Duong, T.-J. King Liu, B. Nikolic, University of California, Berkeley, USA

Distributions of read and write noise margins in large CMOS SRAM arrays are investigated by directly measuring the bit-line current during bitline / wordline (write) or cell supply (read) voltage sweep in a 768Kb 7M1P 45nm CMOS SRAM test-chip. Good correlation between the margins estimates through bitline current measurements and the conventional DC margin measurements in small on-chip SRAM macros with wired-out storage nodes is demonstrated.

5.2 – 3:50 p.m.
Characterization of Bit Transistors in a Functional SRAM, X. Deng, W.K. Loh, B. Pious, T.W. Houston, L. Liu, B. Khan, D. Corum, J. Raval, J. Gertas, F.-Y. Rousey, J. Steck, C. Suwannakinthorn, R. McKee, Texas Instruments, USA

A direct bit transistor access (DBTA) scheme is proposed and implemented in 8Mb SRAMs at 65nm and 45nm nodes. It allows, for the first time, characterization of each bit transistor in a functional SRAM. It thus enables (a) collection of transistor data across bit arrays, (b) collection of massive data for statistical analysis such as on transistor mismatch and NBTI Vt drift, and (c) collection of data for fast failure analysis. Measured data are presented.

5.3 – 4:15 p.m

A 0.7V Single-Supply SRAM With 0.495um^2 Cell In 65nm Technology Utilizing Self-Write-Back Sense Amplifier And Cascaded Bit Line Scheme, K. Kushida, A. Suzuki, G. Fukano, A. Kawasumi, O. Hirabayashi, Y. Takeyama, T. Sasaki, A. Katayama, Y. Fujimura,. T. Yabe, Toshiba Corporation, Japan

A novel SRAM architecture with a high density cell in low supply voltage operation is proposed. A self-write-back sense amplifier realizes cell failure rate improvement by more than two orders of magnitude at 0.6V. A cascaded bit line scheme saves additional process cost for hierarchical bit line layer. A test chip with 256kb SRAM utilizing 0.495µm2 cell in 65nm CMOS technology demonstrated 0.7V single supply operation.

5.4 – 4:40 p.m.

PVT-Variations and Supply-Noise Tolerant 45nm Dense Cache Arrays with Diffusion-Notch-Free (DNF) 6T SRAM Cells and Dynamic Multi-Vcc Circuits, M. Khellah, N.S. Kim, Y. Ye, D. Somasekhar, T. Karnik, N. Borkar, F. Hamzaoglu, T. Coan, Y. Wang, K. Zhang, C. Webb, V. De, Intel, USA

PVT-tolerant and supply noise tracking word-line under-drive circuit, PMOS pass device, and dynamic voltage collapse enable read and write stable Diffusion-Notch-Free (DNF) 6T SRAM cells. Measurements from a 45-nm test-chip show 26X reduction in number of single bit failures using those schemes.

SESSION 6 – TAPA III
Wireline Signal Conditioning

Wednesday, June 18, 3:25 p.m.
Chairpersons: J. Wieser, National Semiconductor
H. Yamada, Oki Electric Industry Co., Ltd.

6.1 – 3:25 p.m.

A 70dB MTPR Integrated Programmable Gain/Bandwidth 4th-Order Chebyshev Highpass Filter for ADSL/VDSL Receivers in 65nm CMOS, F. Lin, X. Yu, S. Ranganathan, T. Kwan, Broadcom Corporation, USA

This paper presents a 4th-order Chebyshev HPF in 65nm CMOS process with programmable gain and corner frequency to support ADSL and 5/6 band VDSL applications. The HPF improves noise performance by applying capacitive feedback and feedforward in the filter. It achieves a 70dB MTPR and -161dBm/Hz (2.8nV/ÖtHz) input referred noise for ADSL mode. An IM3 of -80dBc at 10MHz is measured for VDSL mode.

6.2 – 3:50 p.m.

A 40Gb/s Low-Power Analog Equalizer in 0.13µm CMOS Technology, J.-H. Lu, K.-H. Chen, S.-I. Liu, National Taiwan Univ., Taiwan

A 40Gb/s low-power analog equalizer has been realized in 0.13µm CMOS technology. To achieve a peaking gain of 10dB at 20GHz and low power dissipation, an inductive feedback stage is proposed. This inductive feedback stage consumes 3.6mW from a 1.2V supply and the whole equalizer consumes 14.4mW. The chip occupies 0.57×0.44mm2. For a 40Gb/s PRBS of 27-1, the measured BER is less than 10-12 and the measured maximum peak-to-peak jitter is 12.6ps.

6.3 – 4:15 p.m.
A Merged CMOS Digital Near-End Crosstalk Canceller and Analog Equalizer for Multi-Lane Serial-Link Receivers, J.-H. Lu, K.-H. Chen, A.-M. Lee*, T.-Y. Wu*, S.-I. Liu, National Taiwan University, *Realtek Semiconductor Corp., Taiwan

A digital near-end crosstalk (NEXT) canceller merged with an analog equalizer for multi-lane serial-link receivers has been realized in 0.13µm CMOS technology. With the proposed sign-sign block least-mean-square (SSB-LMS) circuit, a 5Gb/s PRBS of 231-1 suffered from both the channel loss and NEXT for 10-inch FR4 traces is successfully equalized. The measured BER is 10-12 and the measured maximum peak-to-peak jitter is 49.7ps. This chip occupies 0.56×0.76mm2 and consumes 177mW including buffers from a 1.2V supply.

6.4 – 4:40 p.m.
A 12-Gb/s 11-mW Half-Rate Sampled 5-Tap Decision Feedback Equalizer with Current-Integrating Summers in 45-nm SOI CMOS Technology, T. Dickson, J. Bulzacchelli, D. Friedman, IBM T.J. Watson Res. Ctr, USA

The design and experimental results of a low-power, low-area 5-tap DFE implemented in 45-nm SOI CMOS technology are reported. The DFE employs a low-power current-integrating summer with sampling front-end, which eliminates systematic loss inherent in conventional integrating serial receivers. The use of a direct-feedback architecture and CMOS-style rail-to-rail clocking achieves further power and area savings. The 5-tap DFE core occupies 73µm x 50µm and consumes 11 mW from a 1V supply when equalizing 12-Gb/s data passed over a 30" channel with 15dB of loss at 6 GHz.

SESSION 7 – TAPA II
Clocking and Signaling

Thursday, June 19, 8:30 a.m.
Chairpersons: K. Shepard, Columbia University
K. Nose, NEC Corporation

7.1 – 8:30 a.m.

Next Generation Intel® Micro-architecture (Nehalem) Clocking Architecture, N. Kurd, J. Douglas, P. Mosalikanti, R. Kumar, Intel Corporation, USA

This paper describes the Next generation Intel® micro-architecture (Nehalem) 45nm IA processor's Core and I/O clocking architecture. Among the highlights are: configurable clocking, fast-lock low-skew PLLs, high reference clock frequencies, analog supply tracking system, adaptive frequency clocking, low jitter Intel® QuickPath interconnect and Intel® QuickPath memory controller clock generation, and jitter-attenuating DLLs.

7.2 – 8:55 a.m.
A Small-Delay Defect Detection Technique For Dependable LSIs, K. Noguchi, K. Nose, T. Ono*, M. Mizuno, NEC Corporation, *NEC Electronics Corporation, Japan

As continuous process scaling produces large-scale chips, small-delay defects become one of the major chip-reliability limiters. Small-delay defect detection techniques for LSI screening have been developed, which can successfully detect outlier chips among normally-distributed chips in a short testing time. In our experiments with 90nm CMOS 100MHz test chips, we have successfully detected around 1-ns path delay shift caused by small-delay defects in only 1/25 of testing time.

7.3 – 9:20 a.m.
Sensor Data Retrieval Using Alignment Independent Capacitive Signaling, Y.-S. Lin, D. Sylvester, D. Blaauw, University of Michigan, USA

We propose a capacitive coupling based method for sensor data retrieval which can be easily integrated with miniature sensor nodes of sub-mm scale. An alignment independent mechanism is implemented to achieve <15% difference in achievable data rate when the sensor chip is randomly dropped on the data retrieval chip regardless of alignment. To enable passive operation of the sensor chip, the data retrieval chip send power to/receive signal from the sensor chip simultaneously.

7.4 – 9:45 a.m.
Characterizng Sampling Aperture of Clocked Comparators, M. Jeeradit, J. Kim, B. Leibowitz, P. Nikaeen*, V. Wang**, B. Garlepp^, C. Werner, Rambus Inc., *Stanford University, **University of California, Los Angeles, ^SiTime Corp, USA

Practical simulation and measurement methods based on impulse sensitivity functions to characterize the sampling aperture of clocked comparators are demonstrated on a 90nm CMOS testchip. The results comparing a StrongARM latch and a CML latch suggest that the StrongARM latch has a narrower aperture of 23ps but its aperture center is more sensitive to supply (65ps/V). The CML latch has a higher sampling gain of 88.8dB but a lower bandwidth of 6.8GHz.

10:10 a.m. Break

SESSION 8 – TAPA III
Data Converters and Biomedical Circuits

Thursday, June 19, 8:30 a.m.
Chairpersons: L. Breems, NXP Semiconductors
M. Ito, Renesas Technology Corporation

8.1 – 8:30 a.m.
A 1.2V 30mW 8b 800MS/s Time-Interleaved ADC in 65nm CMOS, W.-H. Tu, T.-H. Kang, MediaTek Inc. Taiwan

An 8-bit 800MS/s time-interleaved pipeline ADC with SNDR of 47.8dB and 44.2dB for 1MHz and 400MHz inputs is presented. The techniques of Sub-ADC preamp sharing and reference voltage buffer current-reusing are proposed to minimize power consumption. The ADC implemented in 65nm digital CMOS process with an active area of 0.12mm2 consumes 30mW from a 1.2V supply and achieves a FOM of 0.28pJ/conversion-step.

8.2 – 8:55 a.m.
A 1.2V 250mW 14b 100MS/s Digitally Calibrated Pipeline ADC in 90nm CMOS, H. Van de Vel, B. Buter, H. van der Ploeg, M. Vertregt, G. Geelen, E. Paulus, NXP Semiconductors, The Netherlands

A 14b pipeline ADC is realized in 90nm CMOS at a 1.2V supply. Enabling techniques are range-scaling in the first pipeline stage with charge-reset and digital background calibration of non-linearity. The ADC achieves 73dB SNR and 91dB SFDR at 100MS/s sampling rate and 250mW power consumption. The 73dB SNDR performance is maintained within 3dB up to a Nyquist input frequency and the FOM is 0.7pJ/conv.

8.3 – 9:20 a.m.
A 64 Channel Programmable Closed-loop Deep Brain Stimulator with 8 Channel Neural Amplifier and Logarithmic ADC, J. Lee, H.-G. Rhew, D. Kipke, M. Flynn, University of Michigan, USA

We describe a 64 channel closed-loop deep brain stimulator IC for use in research and treatment of Parkinson's disease. The system generates programmable stimulation currents and senses and filters neural activity recorded with an 8 channel preamplifier and 200kS/s 8bit logADC. The entire system implemented in 0.18μm CMOS, occupies 2.67mm2, and consumes 271μW from a 1.8V supply. In-vivo test data is presented.

8.4 – 9:45 a.m.
A 1-V 450-nW Fully Integrated Biomedical Sensor Interface System, X. Xu, X. Zou, L. Yao, Y. Lian, National University of Singapore, Singapore

This paper presents a 1-V 450-nW fully integrated bio-signal acquisition IC in 0.35-μm CMOS technology which includes a tunable band-pass filter, a variable gain amplifier, and a 12-bit ADC. The ultra-low power is achieved by using an energy-efficient system architecture and a novel tunable band-pass filter. The measurement shows that the overall system draws only 445-nA current from a 1-V supply in the detection mode and 895-nA in the diagnosis mode for electrocardiogram (ECG) applications.

10:10 a.m. Break

SESSION 9 – TAPA II
Frequency Synthesis Components

Thursday, June 19, 10:25 a.m.
Chairpersons: A. Amerasekera, Texas Instruments
J. Lee, National Taiwan University

9.1 – 10:25 a.m.
An Efficient High-Resolution 11-Bit Noise-Shaping Multipath Gated Ring Oscillator TDC, M. Straayer, M. Perrott, Massachusetts Institute of Technology, USA

An 11-bit, 50-Msps time-to-digital converter (TDC) using a multipath gated ring oscillator (GRO) with 6ps of delay per stage achieves low power (2.2 to 21mW) and small area of 160x260µm in 0.13µm CMOS. The structure also achieves first order noise shaping of the GRO quantization and mismatch noise; the resulting TDC error integrates to < 100 fs (rms) in a 1 MHz bandwidth to achieve dynamic range of over 90dB with no calibration required.

9.2 – 10:50 a.m.
Digital Frequency Detector based on Multiphase Ring Oscillator, C.-Y. Cha, M. Lee*, J. Lee, T. Kim, Samsung Advanced Institute of Technology, Korea, *University of California, Los Angeles, USA

A new high resolution digital frequency detector architecture based on multiphase ring oscillator is proposed, and it uses the time resolution of fast-operating deep sub-micron MOS transistor. The proposed DFD is implemented with 65nm CMOS technology. The measured frequency resolution is amount to 75dBc with 10.2MHz input signal. Fabricated digital frequency detector draws about 4mA in 1.2V supply voltage.

9.3 – 11:15 a.m.
93.5~109.4GHz CMOS Injection-Locked Frequency Divider With 15.3% Locking Range, L.-C. Cho, K.-H. Tsai, C.-C. Hung, S.-I. Liu, National Taiwan University, Taiwan

A distributed-LC injection-locked frequency divider is proposed. This frequency divider has been realized in 65nm CMOS technology. The core area is 0.036mm2. The measured operation range is 93.5~109.4GHz. Its center frequency is 102GHz and the locking range is 15.3%. Its power is 5.5mW from the supply of 1.1V.

9.4 – 11:40 a.m.
A 2.5-GHz 860µW Charge-Recycling Fractional-N Frequency Synthesizer in 130nm CMOS, D. Park, W. Lee, S. Jeon, S.H. Cho, KAIST, Korea

A 1.2V 2.5GHz 860µW fractional-N synthesizer is implemented in 130nm CMOS. It employs charge recycling technique for implicit DC-DC conversion without using any voltage regulators, and achieves -77dBc/Hz and -113.5dBc/Hz of phase noise at 100kHz and 1MHz offset, respectively. Self-biased divider and VCO enables robust operation of the proposed circuit.

12:05 p.m. Lunch

SESSION 10 – TAPA III
Multi-Standard RF

Thursday, June 19, 10:25 a.m.
Chairpersons: J. Dawson, Massachusetts Institute of Technology
S. Mutoh, NTT Corporation

10.1 – 10:25 a.m.
A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS, R. Shrestha, R. van der Zee, A. de Graauw*, B. Nauta, University of Twente, *NXP, The Netherlands

A wideband modulator for a 20MHz bandwidth polar modulated PA is presented which achieves a maximum efficiency of 87.5% and a small signal -3dB bandwidth of 285MHz. Realized in 65nm CMOS, it consists of a cascoded nested Miller compensated linear amplifier and a class D switching amplifier. It can deliver 22.7dBm output power to a 5.3W load. With a switching frequency of 118MHz, the output switching ripple is 4.3mVrms.

10.2 – 10:50 a.m.
A Multi-Mode Multi-band CMOS Direct-Conversion Mobile-TV Tuner for DVB-H/T and T-DMB/DAB Applications, M.-W. Hwang, M. Ahn, S. Beck, J.-C. Lee, S. Hong, S. Lee, S. Jeong, S. Lim, H. Cho, Y.-J. Kim*, I.-C. Hwang**, J. Kim, Future Communications IC Inc., *Korea Acrospace University, **Kangwon National University, Korea

A fully integrated direct-conversion mobile-TV tuner for DVB-H/T and T-DMB/DAB applications was fabricated using 0.18μm CMOS process. This tuner has the good SNR and immunity performance over wide dynamic range for multi-band and multi-mode applications with the automatic gain control and calibration schemes. The power consumption is 127mW for VHF and UHF, and 135mW for L-band at 1.8V supply voltage.

10.3 – 11:15 a.m.
A Quad Band WCDMA Transceiver with Fractional Local Divider, H. Kamizuma, T. Yamawaki, Y. Akamine, K. Maeda, S. Tanaka, K. Hikasa*, Hitachi Central Research Laboratory, *Renesas Technology

We developed a quad band (1, 6, 9, and 11) WCDMA transceiver with digital interface. The developed transceiver uses a 2/5 divider in the local part of the direct conversion architecture. Using the 2/5 divider, reduces the number of local synthesizers to only one in the architecture and avoid VCO pulling phenomena of the local synthesizer perfectly. This transceiver achieved 3% EVM and -46 dB ACLR, which is enough of a margin for standard specifications.

10.4 – 11:40 a.m.
All-Digital Out-phasing Modulator for a Software-Defined Transmitter, M. Heidari, M. Lee, A. Abidi, University of California, Los Angeles, USA

An all-digital out-phasing transmitter suitable for software-defined radio (SDR) is presented. It uses a phase-locked loop followed by two digital phase rotator blocks embedded in two delay-locked loops. The chip is fabricated in a 90nm CMOS process with total active area of 3mm2, and tested for GSM and WCDMA standards. The whole transmitter excluding phase-to-digital converter (PDC) consumes 55mA, and the current consumption of the PDC is 70mA.

12:05 p.m. Lunch

SESSION 11 – TAPA II
Processors for HDTV

Thursday, June 19, 1:30 p.m.
Chairpersons: B. Nikolic, University of California, Berkeley
H. Kabuo, Matsushita Electric Ind. Co., Ltd.

11.1 – 1:30 p.m.
A 256mW Full-HD H.264 High-Profile CODEC Featuring Dual Macroblock-Pipeline Architecture in 65nm CMOS, K. Iwata, S. Mochizuki, T. Shibayama, F. Izuhara, H. Ueda, K. Hosogi*, H. Nakata*, M. Ehama*, T. Kengaku, T. Nakazawa, H. Watanabe, Renesas Technology Corp., *Hitachi Ltd., Japan

A video-size-scalable H.264 High-Profile CODEC including 19 specific CPUs for extensibility to multiple standards has been fabricated in 65nm CMOS. With two parallel pipelines for macroblock processing, the CODEC consumed 256mW in real-time encoding of full-HD (1080i) video at an operating frequency of 162MHz. It represents a 38% reduction in power consumption per pixel compared with state-of-the-art designs.

11.2 – 1:55 p.m.
An H.264/AVC Scalable Extension and High Profile HDTV 1080p Encoder Chip, Y.-H. Chen, T.-D. Chuang, Y.-J. Chen, C.-T. Li, C.-J. Hsu*, S.-Y. Chien, L.-G. Chen, National Taiwan University, *UMC, Taiwan

The first single-chip H.264/AVC HDTV 1080p encoder for scalable extension (SVC) with high profile is implemented on a 16.76mm2 die with 90nm process. It dissipates 349/439mW at 120/166MHz for high profile and SVC encoding. The proposed frame-parallel architecture halves external memory bandwidth and operating frequency. Moreover, the prediction architecture with inter-layer prediction tools are applied to further save 70% external memory bandwidth and 50% internal memory access.

11.3 – 2:20 p.m.
An H.264/AVC High422 Profile and MPEG-2 422 Profile Encoder LSI for HDTV Broadcasting Infrastructures, K. Nitta, M. Ikeda, H. Iwasaki, T. Onishi, T. Sano, A. Sagata, Y. Nakajima, M. Inamori, T. Yoshitome, H. Matsuda, R. Tanida, A. Shimizu, J. Naganuma, K. Nakamura, Nippon Telegraph and Telephone Corporation, Japan

An H.264/AVC High422 profile encoder LSI has been developed for HDTV broadcasting infrastructures. It contains 257GOPS ME/MC engines with search ranges of -271.75 to +199.75 (H), -109.75 to +145.75 (V), that support almost all H.264/AVC ME/MC tools. Our evaluations show that it can encode fast moving scenes with 1.2 to 1.7dB higher than the JM. It was successfully fabricated in a 90nm 9level metal CMOS technology with 140 million transistors.

11.4 – 2:45 p.m.

A 2/4/8 Antennas Configurable Diversity OFDM Receiver For Mobile HDTV Application, T. Wada, T. Iida**, H. Mizutani*, S. Sakaguchi*, S. Murakami*, A. Shimizu**, University of the Ryukyus, *Magna Design Net, Inc., **Sanyo Electric Co., Japan

Two array antennas and one carrier diversity combiners are integrated with Japan Terrestrial digital TV (ISDB-T) OFDM receiver using 90nm 7M1P CMOS process. A 2/4/8 antennas diversity receiver can be configured and the low cost 4 antennas diversity reception system can be realized by one LSI. The mobile reception performance is increase by 63% using de-noise filter circuit and SPLINE interpolator. The die area is 49mm2 and the power consumption is 310mW.

3:10 p.m. Break

SESSION 12 – TAPA III
PLLs and Wireless Transceivers

Thursday, June 19, 1:30 p.m.
Chairpersons: C.-M. Hung, Texas Instruments
M. Ikeda, University of Tokyo

12.1 – 1:30 p.m.

A Low Noise, Wideband Digital Phase-Locked Loop Based On A New Time-To-Digital Converter With Subpicosecond Resolution, M. Lee, M. Heidari, A. Abidi, University of California, Los Angeles, USA

A digital PLL uses a high resolution coarse-fine Time-to-Digital Converter (TDC) for wide loop bandwidth. The loop bandwidth is set to 400 kHz with a 26 MHz reference for GSM. The in-band phase noise contribution from the TDC is -116 dBc/Hz, the phase noise is -117 dBc/Hz at high-band 400 kHz offset, and the RMS phase error is 0.3°.

12.2 – 1:55 p.m.

A 0.4ps-RMS-Jitter 1-3GHz Ring-Oscillator PLL using Phase-Noise Preamplification, Z. Cao, Y. Li*, S. Yan, University of Texas at Austin, *Analog Devices, USA

A 1-3GHz tunable multiply-by-8 PLL is implemented in 0.13μm CMOS and occupies 0.07mm2. A proposed fully-differential Gm-C loop filter structure decouples reference spur performance from charge-pump current matching and loop filter leakage, while enables phase error preamplification to lower PLL in-band noise without reducing VCO analog tuning range or increasing loop filter capacitor size. It achieves <-118dBc/Hz PLL in-band noise (>100kHz offset) and 0.4ps-rms jitter (integrated from 3kHz to 300MHz offset) for ≥2.5GHz outputs.

12.3 – 2:20 p.m.
RF Transceiver and Wireless Calibration of On-Chip Frequency Reference for a True Single Chip Radio, Y. Ding, Y. Su, C. Cao, J.-J. Lin, T. Wu, M. Hwang, R. Fox, J. Brewer, K. O, University of Florida, USA

An RF transceiver for operation near 24GHz with an onchip antenna, fractional-N synthesizer and other RF and analog baseband circuits is demonstrated in 130-nm CMOS. A 5-m wireless link was demonstrated using a transceiver pair. A technique for wireless calibration of an on-chip frequency reference is also demonstrated.

12.4 – 2:45 p.m.
A 100Mbps, 0.41mW, DC-960MHz Band Impulse UWB Transceiver in 90nm CMOS, L. Liu, Y. Miyamoto, Z. Zhou, K. Sakaida, R. Jisun, K. Ishida, M. Takamiya, T. Sakurai, University of Tokyo, Japan

A low power impulse ultra-wideband (UWB) transceiver for DC-960MHz band is proposed in this paper. It features a digital pulse-shaping transmitter, a DC power-free pulse discriminator and an error-recovery phase-frequency detector. The developed transceiver in 90nm CMOS achieves the lowest energy consumption of 2.2pJ/bit (TX) and 1.9pJ/bit (RX) at 100Mbps.

3:10 p.m. Break

SESSION 13 – TAPA II
Low Power Memory and Interface Techniques

Thursday, June 19, 3:25 p.m.
Chairpersons: O. Jungroth, Intel Corporation
K. Kajigaya, Elpida Memory, Inc.

13.1 – 3:25 p.m.
A Fully Logic-Process-Compatible, 3-Transistor, SESO-memory Cell Featuring 0.1-FIT/Mb Soft Error, 100-MHz Random Cycle, and 100-ms Retention, N. Kameshiro, T. Watanabe, T. Ishii, T. Mine, T. Sano*, H. Ibe, S. Akiyama, K. Yanagisawa**, T. Ipposhi**, T. Iwamatsu**, Y. Takahashi**, Hitachi Ltd., *Renesas Northern Japan Semiconductor Inc., **Renesas Technology Corp., Japan

A 1-kb memory-cell array composed of single-electron shut-off (SESO) cells was fabricated with the 90-nm logic process for the first time. It features a 0.1-FIT/Mb soft error, 100-MHz random cycle, and 100-ms retention. In addition to a logic-compatible cell structure and a write-data caching scheme, a backup latch circuit with SESO transistors for logic application was also proposed.

13.2 – 3:50 p.m.
Novel Co-design of NAND Flash Memory and NAND Flash Controller Circuits for Sub-30nm Low-Power High-Speed Solid-State Drives (SSD), K. Takeuchi, University of Tokyo, Japan

Three new circuit technologies, selective bit-line precharge scheme, advanced source-line programming, and intelligent interleaving are proposed. By co-designing NAND flash memory and NAND controller circuits, both NAND and the NAND controller are best optimized. The operation current of the NAND flash memory decreases by 60% and 2.5 times as many NAND chips in SSD can operate simultaneously. At sub-30nm generation, the SSD performance improves by 150% without a cost penalty or circuit noise.

13.3 – 4:15 p.m.

A 16Gb/s/link, 64GB/s Bidirectional Asymmetric Memory Interface Cell, K. Chang, H. Lee, J.-H. Chun, T. Wu, T.J. Chin, K. Kaviani, J. Shen, X. Shi, W. Beyene, Y. Frans, B. Leibowitz, N. Nguyen, F. Quan, J. Zerbe, R. Perego, F. Assaderaghi, Rambus Inc., USA

An asymmetric memory interface cell with 32 bidirectional data and four unidirectional request links operating at 16Gb/s per link is implemented in TSMC 65nm CMOS technology. Timing adjustment and equalization circuits for both memory read and write are on the controller to reduce memory cost. Each link operates at a maximum rate of 16Gb/s with comparable margins in both directions at a BER of 10-12. The measured energy efficiency for the cell is 13mW/Gb/s.

13.4 – 4:40 p.m.

A 16-Gb/s Differential I/O Cell with 380fs RJ in an Emulated 40nm DRAM Process, N. Nguyen, Y. Frans, B. Leibowitz, S. Li, R. Navid, M. Aleksic, F. Lee, F. Quan, J. Zerbe, R. Perego, F. Assaderaghi, Rambus Inc., USA

This paper describes a 16-Gb/s differential bidirectional I/O transceiver cell in an emulated 40nm DRAM process. The transceiver implements several techniques to achieve low jitter despite the slow process and constrained power consumption. The transceiver has measured random jitter of 380fs rms at the transmitter output and BER < 10-14 while consuming 8mW/Gb/s.

SESSION 14 – TAPA III
Power Management Circuits and Image Sensor

Thursday, June 19, 3:25 p.m.
Chairpersons: T. Kwan, Broadcom Corp.
M. Igarashi, Sony Corp.

14.1 – 3:25 p.m.

Single-Inductor Dual-Output DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices, M.-H. Huang, K.-H. Chen, W.-H. Wei*, National Chiao Tung University, *Richtek Technology Corp., Taiwan

A peak-current control single-inductor dual-output (SIDO) DC-DC converter is proposed. The proposed SIDO DC-DC converter not only provides dual output sources (one buck and one boost outputs) but also has minimized cross

regulation. Besides, a new hysteresis mode decided by a power decision circuit can effectively prevent SIDO converter from oscillating when power of buck is larger than that of boost. SIDO converter achieves high conversion efficiency at light loads. Experimental results show a high efficiency from 85% at light loads to 94% at heavy loads.

14.2 – 3:50 p.m.
Adaptive Step-Down Switched-Capacitor Power Converter with *z*-Domain Observation-Based Line-Load Regulation, M. Song, I. Chowdhury, D. Ma, A.P. Brokaw*, University of Arizona, *Analog Devices, USA

The paper presents an integrated switched-capacitor power converter, employing an efficient step-down conversion power stage and a cost-effective observation-based controller. The complete z-domain design makes system modeling and analysis consistent and efficient. With an adjustable output voltage range from 1.25 to 2.0V, the converter delivers up to 220mW power from a 3.3 V input source with a maximum efficiency of 74.1%, surpassing a linear regulator's theoretical limit.

14.3 – 4:15 p.m.
An SC Voltage Regulator with Novel Area-Efficient Continuous Output Regulation by Dual-Branch Interleaving Control Scheme, F. Su, W.-H. Ki, C.-Y. Tsui, Hong Kong University of Science and Technology, Hong Kong

A 1.8V to 3.3V SC voltage regulator is present. The dual branches operate in an interleaving fashion for sake of area-efficient continuous output regulation. Therefore the output voltage can be continuously regulated with small ripples. The design was fabricated in 0.35μm CMOS process. A maximum output ripple of 10mV is maintained for loading from 10mA to 180mA. Meanwhile load regulation of 0.0043%/mA and load transient of less than 25us for 150mA current step are measured.

14.4 – 4:40 p.m.
A Very Low Column FPN and Row Temporal Noise 8.9M-Pixel, 60 fps CMOS Image Sensor with 14bit Column Parallel SA-ADC, S. Matsuo, T. Bales, M. Shoda, S. Osawa, B. Almond*, Y. Mo**, J. Gleason**, T. Chow**, I. Takayanagi, Micron Japan Ltd., Japan, *Micron Europe, United Kingdom, **Micron Technology, USA

A 1.25-inch optical format, 8.9M-pixel CMOS image sensor that employs a 4T pinned photodiode (P-PD) pixel and 14bit column ADCs is reported. A 14bit or 12bit digital video signal is streamed out via 16-lane low-voltage, low-power differential serial output ports in 50fps and 60fps operations, respectively. Temporal noise floor of 2.8e-rms and linear full-well of 27.8ke- were obtained at 60 fps operation. Row temporal noise and column FPN are as small as 0.31 e-rms and 0.36 e-rms, respectively.

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 17
8:00 p.m – 10:00 p.m.

Organizers:

Circuits	**Technology**
G. Lehmann, Infineon	T. Grider, Texas Instruments
K. Arimoto, Renesas	Y. Omura, Kansai University

RJ1: Ten years after – Has SOI finally arrived?
Tapa I

Moderators: L. Counts, LC Consulting
K. Ishimaru, Toshiba America

Ten years after introduction of SOI into a production as a competitor to bulk-CMOS, both technologies continue to co-exist in some of the application domains, such as microprocessors and gaming. On the other hand, mainstream SoC's exclusively use bulk-CMOS. A panel similar to this one 10 years ago has concluded that SOI has a performance advantage over bulk, and the cost will be its main barrier for wide adoption. Has anything changed and will it change in the next decade? Will SOI penetrate more market segments or disappear? Does further technology scaling require the migration to fully-depleted SOI?

Panelists:

M. Bohr, Intel	R. Mahnkopf, Infineon
G. Shahidi, IBM	C. Mazure, SOITEC
E. Suzuki, AIST	D. Scott, TSMC
A. Kameyama, Toshiba	M. Usami, Hitachi

CIRCUITS RUMP SESSION
Thursday, June 19
8:00 p.m. – 10:00 p.m.

Organizers: B. Nikolic, University of California, Berkeley
T. Sekiguchi, Hitachi, Ltd.

R1: Photons vs. Electrons – Which Will Win and When? (The Ongoing Race for Short-Distance High-Speed Data Connectivity)
Honolulu I
Organizers: J. Savoj, Qualcomm
M. Fukaishi, NEC

Moderator: J. Wieser, National Semicondcutor

This session discusses the utilization of copper and optical interconnects for high-speed chip-to-chip interfaces, along with the emergence of new disruptive technologies. The panel focuses on high-speed short-range and medium-range data connectivity and

issues regarding the design of transceivers for these systems, as well as the roadmap of IOs for future high-performance/low-power/small-form-factor systems.

Panelists:

M. Horowitz, Stanford Universty — I. Young, Intel
J. D'Ambrosia, Force10 Networks — S. Kasturia, Teranetics
H. Tamura, Fujitsu Japan — Y. Ohtomo, NTT Japan

R2: The Future of Silicon Storage – Can Solid State Technologies Take Center Stage?

Honolulu II

Organizers: A. Bhavnagarwala, IBM
S. Ohshima, Toshiba

Moderator: A. Bhavnagarwala, IBM

With the market for storage class memories projected to exceed 500 ExaBytes* by 2012, and NAND Flash and DDR based solid state drives (SSD) already making inroads into the enterprise sector of storage and into niche applications, will the continued scaling of SSD cost enable silicon to take center stage in storage? Or, would Hard Disk Drives, with Heat Assisted Magnetic Recording and Bit Patterned Media - projected to exceed densities of 50 Terabits/in2, continue to dominate as the technology of choice? A panel of experts from across the industry will present their vision of opportunities and limitations of emerging and incumbent storage technologies that can potentially satisfy the mass storage market created by the proliferation of digital content. (*Gartner)

Panelists:

C. Lam, IBM — K. Tsuchiya, Toshiba
K. Quader, SanDisk — K. Kim, Samsung
M. Kryder, Carnegie Mellon — H.-S.P. Wong, Stanford
S. Lai, Ovonyx

SESSION 15 – TAPA I
Power-Aware Circuit Techniques

Friday, June 20, 8:15 a.m.

Chairpersons: J. Barth, IBM Microelectronics
T. Shiota, Fujitsu Laboratories, Ltd.

15.1 – 8:15 a.m.

A Sub-µs Wake-up Time Power Gating Technique with Bypass Power Line for Rush Current Support, K. Kawasaki, T. Shiota, K. Nakayama, A. Inoue, Fujitsu Laboratories Ltd., Japan

A sub-us wake-up power gating technique was developed for low power SOCs. It uses two types of power switches and separated power lines bypassing rush current to suppress power supply voltage fluctuations. We applied this technique to a heterogeneous

dual-core microprocessor fabricated in 90nm CMOS technology. When wake-up time on the 2M-gate scale circuit was set to 0.24us, the supply voltage fluctuation was suppressed to 2.5mV.

15.2 – 8:40 a.m.
Dynamic Voltage Boost (DVB) Method for Improving Power Integrity of Low-Power Multi-Processor SoCs, Y. Kanno, K. Yoshizumi, Y. Yasu, K. Ishibashi, H. Mizuno, Hitachi Ltd., Japan

We propose a dynamic voltage boosting (DVB) method for improving performance by slightly boosting voltage within a withstand voltage. We measured an improvement of 44 % voltage drop with about 10 % area overhead in a 65 nm CMOS. This DVB method combined with a series power gating can be used to achieve high performance for low-cost low-power SoCs in advanced process technology.

15.3 – 9:05 a.m.
Experimental Evaluation of Digital-Circuit Susceptibility to Voltage Variation in Dynamic Frequency Scaling, M. Fukazawa, M. Kurimoto**, R. Akiyama*, H. Takata**, M. Nagata, Kobe University, *Renesas Technology Corp., ** Renesas Design, Japan

Logical operations in CMOS digital integration are highly prone to fail as the amount of power-supply (PS) drop approaches to threshold. PS voltage variation is characterized by built-in noise monitors in a 32-bit microprocessor of 90-nm CMOS technology, in relation with instruction-level programming for logical failure analysis. Experimental measurements demonstrate that the increased susceptibility of processor operation with dynamic frequency scaling (DFS) can be mitigated through PS noise shaping.

15.4 – 9:30 a.m.
A 1.1V 35µm × 35µm Thermal Sensor With Supply Voltage Sensitivity Of 2ºC/10%-Supply For Thermal Management On The SX-9 Supercomputer, E. Saneyoshi, K. Nose, M. Kajita, M. Mizuno, NEC Corporation, Japan

Presented here is a thermal sensor, based on transistor off-leakage current, that allows measurement error of less than 3.1ºC at 90ºC and less than 2ºC at 10% Vdd deviation. For experimental evaluation, 11 thermal sensors, each of which occupied only 35µm × 35µm area, were placed on a chip, and both the location of a hotspot and the overall temperature distribution were successfully measured and agreed with simulation.

9:55 a.m. Break

SESSION 16 – TAPA II
60-120GHz Wireless Receivers

Friday, June 20, 8:15 a.m.
Chairpersons: F. Dai, Auburn University
K. Agawa, Toshiba

16.1 – 8:15 a.m.
A 1Gbps Mixed-Signal Analog Front End for a 60GHz Wireless Receiver, D.A. Sobel, R.W. Brodersen, University of California, Berkeley, USA

A low-power, mixed-signal, baseband analog front end for 60GHz 1Gb/s wireless communications has been implemented in a standard 90nm CMOS process. The receiver is capable of operating under indoor multipath scenarios, resolving channels with up to

32ns multipath delay spread. It uses mixed-signal equalization and carrier recovery in order to minimize the dynamic range requirements of the converter circuitry, resulting in a low power consumption of 55mW.

16.2 – 8:40 a.m.
19.2mW 2Gbps CMOS Pulse Receiver for 60GHz Wireless Communication, A. Oncu, M. Fujishima, University of Tokyo, Japan

A low-power 60GHz pulse receiver has been fabricated for over-Gbps wireless communication by a standard 90nm CMOS process. The receiver consists of a nonlinear detecting amplifier, a limiting amplifier, an offset canceller and a buffer. The measured sensitivity is the average power of -20dBm for millimeter-wave pulses of 60GHz. The power dissipation and maximum data rate of the receiver are 19.2mW and 2Gbps, respectively. These results indicate the possibility of new low-power and ultrahigh-speed wireless communication using millimeter-wave pulses with CMOS implementation.

16.3 – 9:05 a.m.
A Dual-band 61.4~63GHz/75.5~77.5GHz CMOS Receiver in a 90nm Technology, K.-H. Chen, C. Lee, S.-I. Liu, National Taiwan University, Taiwan

A dual-band 61.4~63GHz/75.5~77.5GHz receiver has been realized in a 90nm CMOS technology. It is composed of a broadband low-noise amplifier, RF/IF mixers, and a quadruplicate-locked phase-locked loop. With the dual down- conversion approach, this dual-band receiver achieves a conversion voltage gain of 25.2dB at 62.5GHz and 19.4dB at 77GHz with an input P1dB of -16dBm. It consumes 132mW from a 1.5V supply.

16.4 – 9:30 a.m.
Circuit Performance Characterization of Digital 45-nm CMOS Technology for Applications around 110GHz, R.A. Aroca, A. Tomkins, Y. Doi*, T. Yamamoto*, S.P. Voinigescu, University of Toronto, Canada, *Fujitsu Laboratories Ltd., Japan

The first 50-GHz to 110-GHz downconverter in 45-nm digital CMOS is presented along with the mm-wave characterization of AMOS caractors, inductors, and transformers. The varactor Q is higher than 6, up to 94 GHz. The downconverter gain is 15dB at 111GHz, and is employed as a broadband test vehicle to characterize the optimal noise gifure current density (JOPT) of 45-nm MOSFETs in the 50 GHz to 110 GHz range.

9:55 a.m. Break

SESSION 17 – TAPA I
High Speed Timing Circuits

Friday, June 20, 10:10 a.m.
Chairpersons: S. Tam, Intel Corporation
J.-Y. Sim, POSTECH

17.1 – 10:10 a.m.
Time-to-Digital Converter with Vernier Delay Mismatch Compensation for High Resolution On-Die Clock Jitter Measurement, T. Hashimoto, H. Yamazaki, A. Muramatsu, T. Sato, A. Inoue, Fujitsu Laboratories Limited, Japan

A time-to-digital converter (TDC) utilizing a vernier delay line (VDL) technique has relatively large timing errors when the mismatch of the vernier delay is large. In order to overcome this problem, we propose a technique for compensating the vernier

delay mismatch using multiple ring oscillation measurements of VDL. We verified it using an on-die jitter measurement circuit implemented in 90nm CMOS technology and 0.880ps timing resolution was obtained experimentally.

17.2 – 10:35 a.m.
In-Situ Jitter Tolerance Measurement Technique for Serial I/O, J. Jaussi, G. Balamurugan, J. Kennedy, F. O'Mahony, M. Mansuri, R. Mooney, B. Casper, U.-K. Moon*, Intel Corporation, *Oregon State University, USA

A 10.2-12.5Gb/s CDR incorporating an on-die jitter modulation circuit that enables in-situ jitter tolerance testing is demonstrated in 65nm CMOS. Sinusoidal jitter is introduced into the CDR loop by modulating the control voltage of the LC-VCO and is programmable in amplitude and frequency. The modulation frequency range is 340kHz-104MHz with modulation amplitudes up to 44UIpp. The on-die jitter tolerance measurements correlate to conventional external jitter tolerance results within 10% across a 0.73-23.5MHz range.

17.3 – 11:00 a.m.
Phase Correction of a Resonant Clocking System Using Resonant Interpolators, L.-M. Lee, C.-K.K. Yang, University of California, Los Angeles, USA

Large static phase errors result from injection-locked LC clock buffers due to slight frequency mismatch between the input frequency and the tank's resonant frequency. The paper demonstrates a technique embedding a resonant interpolator into the clock buffer to correct the phase error without additional buffer elements. The test chip is fabricated in a 0.13µm digital CMOS technology. Measured DNL of the resonant interpolator is <0.6LSB even with quadrature inputs and phase error <1ps is achieved.

17.4 – 11:25 a.m.
A Multi Standard 1.5 to 10Gb/s Latch-Based 3-Tap DFE Receiver with a SSC Tolerant CDR for Serial Backplane Communication, M. Pozzoni, S. Erba, P. Viola, M. Pisati, E. Depaoli, D. Sanzogni, R. Brama**, D. Baldi, M. Repossi, F. Svelto*, STMicroelectronics, *Universita degli Studi di Pavia, **Universita di Modena e Reggio Emilia, Italy

A 1.5 to 10Gb/s SATA/SAS/FC receiver in 65nm CMOS is presented. It is based on an adaptive 3-tap latch-based DFE data recovery with self-aligning capability and on an early-late digital clock recovery capable of SSC tracking. Extensive digital features allow self-calibration and eye analysis. The macro measures 0.3mm2 and consumes 140mA from 1V at 8.5Gb/s.

11:50 p.m. Lunch

SESSION 18 – TAPA II
Oversampled Data Converters

Friday, June 20, 10:10 a.m.
Chairpersons: J. Gealow, MediaTek Wireless, Inc.
M. Ito, Renesas Technology Corporation

18.1 – 10:10 a.m.
A 1.3-mW per-Channel 103-dB SNR Stereo Audio DAC with Class-D Head-Phones Amplifier in 65nm CMOS, Y.-H. Lee, C.-K. Seok, B.-J. Kim, S.-B. You, W.-S. Yeum, H.-J. Park, Y.-H. Jun, B.-S. Kong*, J.-W. Kim, Samsung Electronics, *Sungkyunkwan University, Korea

The stereo audio DAC with novel single-ended class-D amplifier achieving a 103-dB SNR is fully integrated in a 65nm CMOS technology. Novel asymmetric pulse-width modulation (PWM) is applied to minimize switching noise and nonlinearity in the class-D amplifier. The adjustable delta-sigma modulator is also used to suppress supply-voltage modulation. All the functions needed for portable audio playback are implemented in a 0.53-mm2 area dissipating only 1.3-mW per channel from a 2.5-V supply.

18.2 – 10:35 a.m.
A 0.7-V 100-dB 870-µW Digital Audio Σ Δ Modulator, H. Park, K. Nam, D. Su, K. Vleugels, B. Wooley, Stanford University, USA

A high-precision, low-voltage, low-power ∑Δ modulator has been designed using a delayed input feedforward architecture and a tracking multi-bit quantizer employing a single comparator. A 0.18-µm CMOS experimental prototype achieves 100 dB of dynamic range, 100-dB peak SNR and 95-dB peak SNDR for a signal bandwidth of 25 kHz, while consuming only 870 µW of total power from a 0.7-V supply at a 5-MHz sampling rate.

18.3 – 11:00 a.m.
A 2.1mW/3.2mW Delay-Compensated GSM/WCDMA Σ Δ Analog-Digital Converter, M. Vadipour, C. Chen, A. Yazdi, M. Nariman, T. Li, P. Kilcoyne, H. Darabi, Broadcom Corporation, USA

A technique to compensate for the harmful excess loop delay in a continuous time ∑Δ analog-digital converter is presented. With no extra power consumption or area penalty the technique is suitable for variety of applications employing continuous time ∑Δ analog-digital converters. This work presents a dual mode ∑Δ ADC for GSM/WCDMA applications with DR of 86dB/63dB for 100KHz/1.92MHz in a 65nm CMOS technology with power consumption of 2.1mW/3.2mW.

18.4 – 11:25 a.m.
A 14b 23MS/s 48mW Resetting Σ Δ ADC with 87dB SFDR 11.7b ENOB & 0.5mm^2 Area, C. Lee, M. Flynn, University of Michigan, USA

A 14b 23MS/s ADC that pipelines a 2nd order resetting SD modulator with a 10b cyclic ADC and requires no front-end S/H is presented. The architecture uses a resetting ∑Δ modulator at the front-end for accuracy and a cyclic ADC at the back-end for residual error quantization. This calibration-free ADC achieves no missing codes, 87dB SFDR and 11.7b ENOB. Fabricated in 0.18µm CMOS with a core area of 0.5mm2, it consumes 48mW from a 2V supply.

11:50 p.m. Lunch

HONOLULU SUITE
2008 Circuits Luncheon
(Separate Registration Required)

Friday, June 20, 12:00 p.m.

The Great Transatlantic Cable and the Birth of Electrical Engineering, Tom Lee, Stanford University

The name Cyrus Field should be much more widely known than it is, particularly among electrical engineers. For we have him to thank for the 19th century's equivalent of the Moon program; the laying of the first transatlantic telegraph cable. Spanning the Atlantic without amplifiers isn't as easy as it sounds. Field's multiple attempts between 1858 and 1866 were punctuated by humiliating failure and the American Civil War. A board of inquiry convened in the aftermath of the first failure, identified several

problems, including Field's near total reliance on a medical doctor for technical advice, as well as a frustrating lack of a technical vocabulary even to describe aspects of the failure itself. The response to this analysis was the creation of the language and profession of electrical engineering with William Thomson, as new technical lead for the project. He was perhaps the first professional electrical engineer. For making the 1866 cable a success, Thomson was knighted that year and eventually became Lord Kelvin. This talk will describe the technical history of the cable project with a focus on how it established electrical engineering as a profession.

To register for the luncheon, please refer to the registration form for fee information.

SESSION 19 – TAPA I
Power-Aware Processing

Friday, June 20, 1:30 p.m.
Chairpersons: V. De, Intel Corporation
M. Hariyama, Tohoku University

19.1 – 1:30 p.m.
A Powerful Yet Ecological Parallel Processing System Using Execution-Based Adaptive Power-Down Control And Compact Quadruple-Precision Assist FPUs, H. Aoki, T. Kawahara, M. Yamaoka, C.Yoshimura, Y. Nagasaka, K. Takayama, N. Sukegawa, Y. Fukumura, M. Nakahata, H. Sawamoto, M. Odaka, T. Sakurai*, K. Kasai, Hitachi Ltd., *University of Tokyo, Japan

We have developed a general-purpose parallel processing system with fine-grained execution-based adaptive power-down control and compact quadruple-precision (QP) assist floating-point execution units (FPUs), and demonstrated it in a test chip. Power could be reduced adaptively down to 52% with these systems and almost twice the performance was achieved in QP addition with only 22% more transistors than conventional double precision Fused Multiply-Add FPUs use.

19.2 – 1:55 p.m.
The Phoenix Processor: A 30pW Platform for Sensor Applications, M. Seok, S. Hanson, Y.-S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, D. Blaauw, University of Michigan, USA

An integrated platform for sensor applications, called the Phoenix Processor, is implemented in a carefully-selected 0.18µm process with an area of 915x915µm2, making on-die battery integration feasible. Phoenix uses a comprehensive sleep strategy with a unique power gating approach, an event-driven CPU with compact ISA, data memory compres-sion, a custom low leakage memory cell,

and adaptive leakage management in data memory. Measurements show that Phoenix consumes 29.6pW in sleep mode and 2.8pJ/cycle in active mode.

19.3 – 2:20 p.m.
An Asynchronous Power Aware and Adaptive NoC Based Circuit, E. Beigne, F. Clermidy, J. Durupt, H. Lhermet, S. Miermont, Y. Thonnart, T. Tran-Xuan, A. Valentian, D. Varreau, P. Vivet, CEA-LETI MINATEC, France

A fully power aware GALS NoC circuit is presented in this paper. The circuit is arranged around an asynchronous NoC providing a 17Gbits/s throughput and automatically reducing its power consumption by activity detection. Both dynamic and static power consumptions are globally reduced using adaptive design techniques applied locally for each NoC units. The dynamic power consumption can be reduced up to a factor of 8 while the static power consumption is reduced by 2 decades in stand-by mode.

19.4 – 2:45 p.m.
DSP Architecture Optimization in Matlab/Simulink Environment, R. Nanda, C.-H. Yang, D. Markovic, University of California, Los Angeles, USA

An automated architecture optimization for DSP algorithms within graphical Matlab/Simulink environment is proposed. The optimization uses Integer Linear Programming for scheduling and retiming of hardware blocks. The high-level block-diagram based Simulink model maps to FPGA or ASIC. Users can control the tuning range of architecture parameters and select solutions from energy-area-performance tradeoff space. The hierarchical method produces optimal architectures with energy efficiency of 5GOPS/mW in a 90nm CMOS technology.

3:10 p.m. Break

SESSION 20 – TAPA II
High Speed Transceivers

Friday, June 20, 1:30 p.m.
Chairpersons: J. Savoj, Qualcomm
J. Lee, National Taiwan University

20.1 – 1:30 p.m.
A 40-Gb/s Transceiver in 0.13-µm CMOS Technology, J.-K. Kim, J. Kim**, G. Kim*, H. Chi, D.-K. Jeong, Seoul National University, Korea, *Silicon Image, **Rambus Inc., USA

A fully integrated 40-Gb/s transceiver is implemented in a 0.13-µm CMOS. This paper describes the challenges in designing a 20-GHz sampler, a 20-GHz quadrature LC-VCO, a 20-GHz bang-bang phase detector, and a 40-Gb/s equalizer. The transceiver dissipates 3.6W from a 1.45-V supply. With the equalizer on, the transmit jitter of the 39-Gb/s PRBS data after the package and board traces is 1.85psrms and the recovered clock jitter is 1.77psrms. The measured BER is <1.0E-14.

20.2 – 1:55 p.m.
A 7.5Gb/s Transmitter with Self-Adaptive FIR, D. Tonietto, J. Hogeboon, E. Bensoudane, S. Sadeghi, H. Khor, P. Krotnev, STMicroelectronics, Canada

This paper presents an adaptation method for transmit multi-tap FIR based on exploration of the receive eye at the far end receiver. This method does not require back-channel or coding overhead and does not involve any proprietary functionality in the far-end SerDes. The proposed method was proven in a CMOS 65n SerDes over a variety of copper media for data-rates up to 9.4 Gbps.

20.3 – 2:20 p.m.
A TeraBit/s-Throughput, SerDes-Based Interface for a Third-Generation 16 Core 32 Thread Chip-Multithreading SPARC Processor, J. Nasrullah, A. Amin, W. Ahmad, Z. Qin, Z. Mushtaq, O. Javed, J. Yoon, L. Chua, D. Huang, B. Huang, M. Vichare, K. Ho, M. Rashid, Sun Microsystems, USA

Third-generation 16 core 32 thread chip-multithreading SPARC processor interface has 1.1Tbps I/O throughput with 112 Tx/176 Rx SerDes channels in 46mm2. Individual links run at BER of 1E-12 on FR4 PCBs at 4.08-0.5Gbps full-half rate, and 18mW/ch/Gbps at 2.67Gbps. Each link has linear equalization, 15 deemphasis and 8 output-swing control settings, and latency of 8UI in Rx and 14-16UI in Tx.

20.4 – 2:45 p.m.
A 21-Channel 8Gb/s Transceiver Macro with 3.6ns Latency in 90nm CMOS for 80cm Backplane Communication, A. Hayashi, M. Kuwata, K. Suzuki, T. Muto, M. Tsuge, K. Nagashima, D. Hamano, T. Usugi, K. Nakajima, M. Ogihara, N. Mikami*, K. Watanabe, Hitachi Ltd., *Hitachi ULSI Systems, Japan

A 21-Channel 8Gb/s transceiver is implemented in a 90nm CMOS technology. 168Gb/s uncoded data transmission with 3.6ns latency is achieved with 4-tap FFE, receiver equalization, jitter tolerant CDR and low jitter PLL. Measured bathtub plots for 80cm FR-4 backplane indicate BER<10-15 with 0.11UI phase margin at the nominal power consumption of 160mW/ch.

3:10 p.m. Break

SESSION 21 – TAPA I
Cache and Embedded Memories

Friday, June 20, 3:25 p.m.
Chairpersons: G. Lehmann, Infineon Technologies
C. Kim, Samsung Electronics Co., Ltd.

21.1 – 3:25 p.m.
A One MB Cache Subsystem Prototype with 2GHz Embedded DRAMs in 45nm SOI CMOS, P. Klim, J. Barth, W. Reohr*, D. Dick, G. Fredeman, G. Koch, H. Le, A. Khargonekar, P. Wilcox, J. Golz, J.B. Kuang*, A. Mathews, T. Luong, H. Ngo, R. Freese**, H. Hunter*, E. Nelson, P. Parries, T. Kirihata, S. Iyer, IBM Systems and Technology Group, *IBM Research Division, **Advanced Micro Devices, USA

We present a 1MB cache subsystem that integrates 2GHz embedded DRAM macros, charge pump circuits, a 4Kb one-time-programmable ROM, clock multipliers, and built-in self test circuitry, having a 36.5GB/s peak system data-rate. The eDRAM employs a programmable pipeline, achieving a 1.8ns latency.

21.2 – 3:50 p.m.
A High Performance 2.4 Mb L1 and L2 Cache Compatible 45nm SRAM with Yield Improvement Capabilities, R. Joshi, R. Houle, D. Rodko, P. Patel, W. Huott, R. Franch, Y. Chan, D. Plass, S. Wilson, S. Wu, R. Kanj, IBM, USA

A fully functional and stable 2.4 Mb L1 and L2 Cache compatible 6T SRAM is demonstrated. Measured results show operation from -40oC to 120oC, speed of 6.5 GHz and 3.8 GHz for L1-Cache cells and L2-Cache cells, respectively, at 1 V and 25oC, with high yield. Key features include multi-setting programmable clock block, separate read/write margin circuitry, low noise dynamic decoders, bit select circuitry supported by newly developed fast Monte Carlo technique.

21.3 – 4:15 p.m.

A 0.6V 45nm Adaptive Dual-rail SRAM Compiler Circuit Design for Lower VDD_min VLSIs, Y.H. Chen, W.M. Chan, S.Y. Chou, H.J. Liao, H.Y. Pan, J.J. Wu, C.H. Lee, S.M. Yang, Y.C. Liu, H. Yamauchi*, TSMC, Taiwan, *Fukuoka Institute of Technology, Japan

A 0.6V 45nm dual-rail SRAM design utilizing an adaptive voltage regulator targeting for an SRAM compiler application is proposed for the first time. To relax IR-drop constraints of CVDD power routings in P&R flow, shifting bite-line (BL) pre-charge power supply from CVDD to VDD is adopted in this work. This also avoids the congestion of the VDD and CVDD power mesh. A 45nm test chip has demonstrated that these concepts successfully can push the VDD_min down to 0.6V, which is > 250mV lower than the conventional single-rail SRAM's.

21.4 – 4:40 p.m.

A 45-nm Single-port and Dual-port SRAM Family with Robust Read/Write Stabilizing Circuitry under DVFS Environment, K. Nii, M. Yabuuchi, Y. Tsukamoto, S. Ohbayashi, Y. Oda*, K. Usui**, T. Kawamura, N. Tsuboi, T. Iwasaki, K. Hashimoto, H. Makino, H. Shinohara, Renesas Technology Corporation, *Shikino High-Tech Corporation, **Daioh Electric Corporation, Japan

We propose an enhanced design solution for embedded SRAM macros under DVFS environment. The improved wordline suppression technique compensates the read stability against process variation, facilitating the Fab. portability. The negative bitline technique expands the write margin for not only 6T single-port (SP) cell but also 8T dual-port (DP) cell even at the 0.7V lower supply voltage. Using 45-nm CMOS technology, we fabricated both SP and DP SRAMs with the proposed circuitry. We achieve robust operations from 0.7V to 1.3V wide supply voltage.

SESSION 22 – TAPA II
Pipelined A/D Converters

Friday, June 20, 3:25 p.m.
Chairpersons: K. Gulati, Cambridge Analog Technologies Inc.
M. Nagata, Kobe University

22.1 – 3:25 p.m.

A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Residue Amplification, J. Hu, N. Dolev, B. Murmann, Stanford University, USA

An ultra-low power pipelined ADC is realized by replacing conventional op-amp circuits with dynamic source-follower gain stages. The presented 90-nm CMOS converter operates at 50MS/s and achieves an SNDR of 49.4dB while dissipating 1.44mW from a 1.2-V supply.

22.2 – 3:50 p.m.

A Fully-Differential Zero-Crossing-Based 1.2V 10b 26MS/s Pipelined ADC in 65nm CMOS, S.-K. Shin, Y.-S. You, S.-H. Lee, K.-H. Moon, J.-W. Kim, L. Brooks*, H.-S. Lee*[1,*2], Samsung Electronics, Korea, *[1]Massachusetts Institute of Technology, USA, *[2]Cambridge Analog Technologies, Inc., USA

A fully-differential zero-crossing-based 10b 26MS/s pipelined ADC in a 65 nm CMOS process is presented. Switched-capacitor overshoot correction is compatible with the differential topology and allows faster operation. A CMFB is engaged in the coarse phase for constant common-mode. The 0.33mm2 ADC achieves 54.3dB SNDR with a FOM of 161fJ/step.

22.3 – 4:15 p.m.
A 12b 50MS/s 10.2mA 0.18µm CMOS Nyquist ADC with a Fully Differential Class-AB Switched OP-AMP, H.-C. Choi, Y.-J. Kim, M.-H. Lee, Y.-L. Kim, S.-H. Lee, Sogang University, Korea

A 12b 50MS/s pipelined ADC based on a fully differential class-AB switched op-amp achieves low power consumption with a high differential input range of 2.4Vp-p. The proposed input sampling network samples wideband signals exceeding the Nyquist frequency without a SHA. The prototype ADC in a 0.18µm CMOS shows a power dissipation of 18.4mW at 50MS/s and 1.8V with an active die area of 0.26mm2.

22.4 – 4:40 p.m.
A Process-Scalable Low-Power Charge-Domain 13-bit Pipeline ADC, M. Anthony, E. Kohler, J. Kurtze, L. Kushner, G. Sollner, Kenet Inc., USA

A 13-bit ADC is implemented using a novel charge-domain architecture. Enhanced bucket-brigade circuitry and a tapered charge pipeline provide precision charge-domain operation in a standard CMOS process, while eliminating the need for signal-path op-amps. The prototype ADC, implemented in 0.18µm CMOS, provides 10.65 ENOB at 250 MS/s while consuming only 140 mW, yielding an exceptionally low FoM of 0.28 pJ/conversion-step. Simulations indicate that the architecture and circuitry are well suited to scaling below 90nm.